DOCUMENT-IDENTIFIER: US 20010007365 A1

TITLE: METHODS OF FABRICATING INTEGRATED CIRCUIT MEMORIES
INCLUDING TITANIUM NITRIDE BIT LINES

--------- KWIC --------- - all Ti N plugs (none in search, not reviewed)

Abstract Paragraph - ABTX (1):

Integrated circuit memory devices include a memory cell field effect transistor in an integrated circuit substrate, a conductive plug that electrically contacts the memory cell field effect transistor and a titanium nitride bit line that electrically contacts the conductive plug opposite the memory cell filed effect transistor. Titanium nitride also may be used to electrically contact field effect transistors in the peripheral region of the integrated circuit memory device. Titanium nitride can be used as a bit line metal instead of conventional tungsten, and as a conductive plug to contact both p.sup.+-type and n.sup.+-type source/drain regions in the peripheral region of the memory device. The titanium nitride conductive plugs and bit lines may be formed simultaneously.

Summary of Invention Paragraph - BSTX (9):

[0007] In order to further reduce the wiring resistance, it is known to employ a metal bit line instead of a conventional polysilicon, silicide or polysilicon/silicide bit line. For example, U.S. Pat. No. 5,407,861 entitled Metalization Over Tungsten Plug describes a plug contact process wherein contact holes are etched and an ohmic/barrier metal layer such as titanium/titanium nitride and a filler metal such as tungsten are blanket deposited. Tungsten hexaflouride (WF.sub.6) is used as a source gas for depositing the tungsten layer. The barrier metal layer is generally very thin, compared to the tungsten contact plug layer which generally is deposited to a thickness of greater than half the contact layer. In particular, the barrier metal layer may have thickness between several tens to several hundred Angstroms. Accordingly, if the barrier metal layer does not function properly, for example due to poor step coverage, particularly at the bottom corner of a contact hole, the fluorine component of the tungsten hexaflouride gas may react
with the titanium component of the barrier metal layer. As a result, an undesirable nonconductive material such as TiF.sub.x may be produced on the contact hole which can increase the contact resistance. Moreover, a lifting between the metal line and the source/drain region 16 also may take place, giving an incomplete electrical connection. Finally, depending on the process

DOCUMENT-IDENTIFIER: US 20020005534 A1

TITLE: Semiconductor memory device and method of manufacturing the same

--------- KWIC --------

Abstract Paragraph - ABTX (1):

According to the present invention, an overlay margin is secured for matching a wiring electrode 11 with a storage electrode 15 of a capacitor at their point of contact and the required area for a memory cell can be decreased by placing the plug electrode 11 of titanium nitride in the active region of a semiconductor substrate or over the gate electrode, reducing the size of the opening for passing the storage electrode 15 of the capacitor of a stacked structure, and decreasing the line width of a wiring electrode 13. By the common use of the above-mentioned plug electrodes in a CMISFET region in the peripheral circuit and in a memory cell of a static RAM, their circuit layouts can be made compact.

Summary of Invention Paragraph - BSTX (29):

[0026] a plurality of first conductors (plug electrodes) passing through the first insulating film and being made of titanium nitride having superior covering properties; and

Detail Description Paragraph - DETX (6):

[0068] Plug electrodes 11 made of titanium nitride are used both in the highly-doped n-type impurity regions 7, 8 and in the highly-doped p-type impurity regions 9. The plug electrode on the highly-doped n-type impurity region 7 of the memory cell is connected to a wiring electrode 13 as the data line. A storage electrode (bottom electrode) 15 of a crown-shaped capacitor is provided above the data line 13. The storage electrode 15 is connected to the plug electrode 11 on the highly-doped n-type impurity region 8, and is electrically connected to the MISFET. In the silicon dioxide film 14 as the inter-layer dielectric, there is formed an opening that is smaller than in diameter than the plug electrode 11, and the storage electrode 15 is connected

DOCUMENT-IDENTIFIER: US 20020006674 A1

TITLE: Hydrogen-free contact etch for ferroelectric capacitor formation

--------- KWIC ---------

Detail Description Paragraph - DETX (6):

[0029] A dielectric layer 112 is formed over the entire substrate and is patterned and etched so as to form openings for contacts to the substrate and gate structures to be formed (step 202). These openings are filled with one or more conductive materials, such as plug 114 (preferably comprised of a metal such as tungsten, molybdenum, titanium, titanium nitride, tantalum nitride, metal silicide such as Ti, Ni or Co, copper or doped polysilicon). A liner/barrier layer may or may not be formed between the plug 114 and dielectric 112. A liner/barrier layer 116 is illustrated in FIG. 1 and is, preferably, comprised of Ti, TiN, TaSiN, Ta, TaN, TiSiN, a stack thereof, or any other conventional liner/barrier material. Preferably, the contacts will be formed so as to land on the silicided regions of the source/drain regions and gate structures.

DOCUMENT-IDENTIFIER: US 20020016273 A1

TITLE: Dilute cleaning composition and method for using same

---------- KWIC ---------

Detail Description Paragraph - DETX (10):

[0026] In the fabrication of a multilevel interconnect structure, a contact hole 18 is typically defined in an insulating layer 20, such as, for example, borophosphosilicate glass (BPSG), as illustrated in FIG. 1A. The contact hole 18 is defined over an active area of an underlying substrate, as represented generally by 22. An interconnect structure 24 is then formed in the contact hole 18 using any suitable materials and methods for forming the same. Typical
interconnect 24 fabrication includes formation of a series of layers, such as, for example, titanium silicide, titanium nitride, and a metal plug or other conductive layers. Next, a blanket layer of metal 26 is deposited over the interconnect structure 24 and insulating layer 20, to produce the structure illustrated in FIG. 1A. The metal layer 26 can be any conductive material, such as, for example, aluminum or aluminum alloyed with copper. Other elements
that can constitute the conductive material include titanium and silicon.

US-PAT-NO: 6020248

DOCUMENT-IDENTIFIER: US 6020248 A

TITLE: Method for fabricating semiconductor device having capacitor increased in capacitance by using hemispherical grains without reduction of dopant concentration

--------- KWIC --------

Detailed Description Text - DETX (27):

Subsequently, the titanium nitride layer 32a is uniformly etched away without an etching mask by using SF.sub.6 gaseous etchant. A titanium nitride plug 32b is left in the contact hole 31b as shown in FIG. 6C. The titanium nitride plug 32b may be annealed in ammonia ambience at 600 degrees to 900 degrees in centigrade so as to make the titanium nitride dense.

Detailed Description Text - DETX (36):

Titanium nitride is deposited to 30 nanometers to 600 nanometers thick over the entire surface of the resultant semiconductor structure by using a sputtering or a chemical vapor deposition, and the titanium nitride layer is patterned into a titanium nitride strip 40d by using the lithographic techniques and the dry etching. The titanium nitride strip 40d covers at least the source region 41c as shown in FIG. 7B. The titanium nitride strip 40d may be increased in dense by using a lamp annealing in nitrogen ambience or ammonia ambience at 600 degrees to 900 degrees in centigrade. Alternatively, titanium is deposited by using a sputtering or a chemical vapor deposition, and the titanium layer may be lamp annealed in the nitrogen ambience or the ammonia ambience at 600 degrees to 900 degrees in centigrade so as to nitride the titanium layer.

Current US Class - CLAS (2):

438

EAST Browser - L12 (84) 10 not 11 | US 6008124 A | Tag S | Doc 45/84 (SORTED) | Format : KWIC

File Edit View Tools Window Help

US-PAT-NO: 6008124

DOCUMENT-IDENTIFIER: US 6008124 A

TITLE: Semiconductor device having improved lamination-structure reliability for buried layers, silicide films and metal films, and a method for forming the same

--------- KWIC ---------

Brief Summary Text - BSTX (15):

Various techniques have been proposed with a view to avoiding the above-noted problem. For instance, Shinriki et al. propose a technique (Ext. Abst. SSDM, p.968, 1994). In the technique, after formation of a connection hole an anneal is carried out in an ambient of NH.sub.3 at a temperature of approximately 850 degrees centigrade without deposition of titanium nitride/titanium film 19, to form a titanium nitride film on top of a titanium silicide film. This is followed by selective deposition of aluminum only in the connection hole by selective CVD.

Current US Class - CLAS (2):

438

DOCUMENT-IDENTIFIER: US 20020072223 A1

TITLE: Method of enhancing adhesion of a conductive barrier layer to an underlying conductive plug and contact for ferroelectric applications

-------- KWIC --------

Detail Description Paragraph - DETX (6):

[0033] A dielectric layer 112 is formed over the entire substrate and is patterned and etched so as to form openings for contacts to the substrate and gate structures to be formed (step 202). These openings are filled with one or more conductive materials, such as plug 114 (preferably comprised of a metal such as tungsten, molybdenum, titanium, titanium nitride, tantalum nitride, metal silicide such as Ti, Ni or Co, copper or doped polysilicon). A liner/barrier layer may or may not be formed between the plug 114 and dielectric 112. A liner/barrier layer 116 is illustrated in FIG. 1 and is, preferably, comprised of Ti, TiN, TaSiN, Ta, TaN, TiSiN, a stack thereof, or any other conventional liner/barrier material. Preferably, the contacts will be formed so as to land on the silicided regions of the source/drain regions and gate structures.

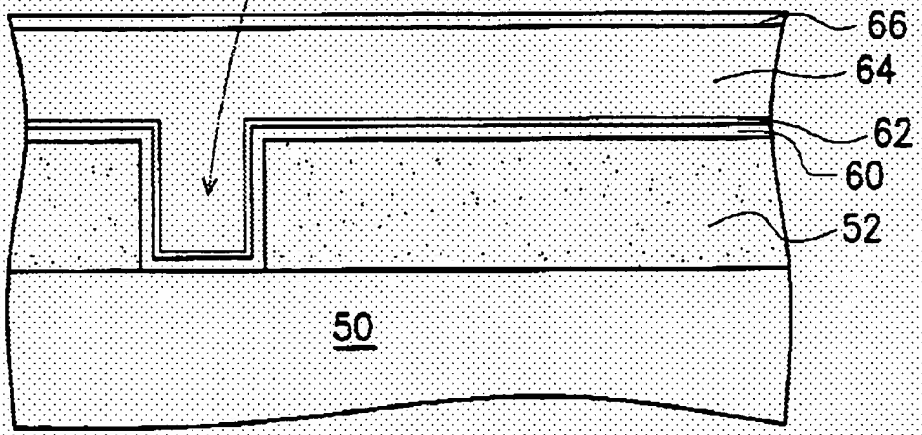
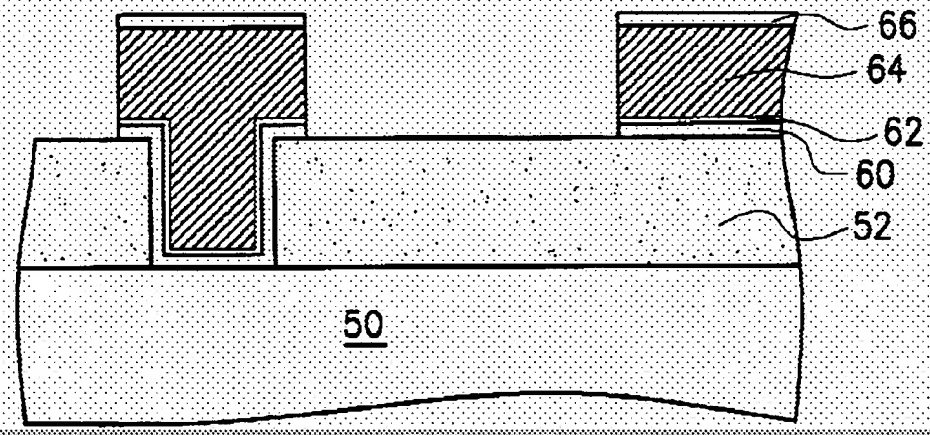


FIG. 3D



titanium nitride layer. Normally, after the barrier layer deposits, either the wafer is exposed to the air for a period of time or a thermal treatment is conducted to increase the insulating ability of titanium nitride. When the thermal treatment is conducted, the titanium at the bottom of the layer and the surface of the silicon substrate form a layer of titanium silicide that decreases the resistance between the conducting structure layer and silicon substrate. Afterwards, a metal layer is deposited on the barrier layer and then an anti-reflective layer is deposited on the metal layer. The

the diffuser/mixer 20. The hydrogen gas is supplied to the diffuser/mixer 20 at a rate of approximately 50 SCCM. A third tube 40 extends through the end cap 14 from a source of ammonia 42 to a position adjacent the diffuser/mixer 20
within the chamber 11 and ammonia gas is supplied therethrough at a rate of approximately 40 SCCM. These flow rates relate to the particular apparatus being used, and will vary with changes in equipment. The preferred ratio of gas flows (by volume), regardless of equipment configuration, for titanium tetrachloride:ammonia:hydrogen is 11:40:50. The ratio of gas flows, titanium tetrachloride, ammonia and hydrogen, should be controlled to within approximately .+-.25% or deposits other than titanium nitride result and a loss of deposition rate and uniformity occurs.

Detailed Description Text - DETX (6):
In an actual operation, 54 wafers were placed in the quartz boat 52 with the approximately 4-5 mm spacing. The flat temperature of the furnace 10 within the chamber 11 across the boat 52 was 700.degree. C. Titanium tetrachloride, ammonia, and hydrogen gas were introduced at the 680.degree. C. point illustrated in FIG. 1. The flow of the gases was controlled so that it was approximately 40 SCCM of ammonia, 11 SCCM of titanium tetrachloride and 50 SCCM
of hydrogen with the pressure in the chamber 11 remaining within the range of 100 to 300 millitorr (13.3-40 Pa). The growth rate of titanium nitride on the wafers was approximately 3.0 to 3.5 nm per minute. A thin layer between 100 and 200 nm was grown. The resistivity of the titanium nitride layer subsequent to deposit was 75 to 100 microohm centimeter. Subsequent to deposition the titanium nitride layer was annealed in situ at a temperature between 900.degree. C. and 1000.degree. C. for approximately 15 minutes in a nitrogen
atmosphere. After annealing the resistivity dropped to 30 to 40 microohm centimeter.

Detailed Description Text - DETX (10):
Thus, a new material, titanium nitride, for use in the formation of gate electrode and interconnects in MOS memories and microprocessors is disclosed.

The materials utilized (titanium tetrachloride in a liquid form, ammonia and hydrogen gas) are very inexpensive. Further, the equipment utilized (a resistance heated furnace) is relatively standard equipment in semiconductor processing plants and requires only minor external modifications. As mentionec

previously, the titanium tetrachloride vapor is obtained from a liquid source and, since the vapor pressure must be relatively constant to provide optimum control, the liquid source volume must be relatively constant. Further, if the

conductive barrier layer **140** comprises one or more materials from the group of: titanium, titanium nitride, tantalum, tantalum nitride, tungsten nitride, ternary metal-silicon-nitride (WSi_xN_y), and ternary metal-boron-nitride (WB_xN_y). Tungsten nitride is especially suited as a seed layer for electroless plating of copper. The conductive barrier layer **140** is preferably deposited to a thickness of between about 500 Angstroms and 5,000 Angstroms.

A metal layer **144** is deposited overlying the conductive barrier layer **140** and filling the trenches, as shown in FIG. **4**. The metal layer **144** may comprise copper, a copper alloy, aluminum, or an aluminum alloy. Preferably, the metal layer **144** comprises copper that has been deposited by one or more of the following processes: physical vapor deposition (PVD), electroless plating, and chemical vapor deposition (CVD). Subsequent annealing of the deposited copper in a furnace or in rapid thermal annealing (RTA) equipment at a temperature of between about 100 degrees C. and 400 degrees C. is performed. Note that the relatively large width of the trench allows the copper layer **144** to be deposited without creating voids.

Referring now to FIG. **5**, another important feature is described. The metal layer **144** and the conductive barrier layer **140** are polished down to confine the metal layer **144** and the conductive barrier layer **140** to the trenches and to thereby form the damascene interconnects. At this point in the process, the interconnect pattern for the interconnect level has been formed in the trenches and has been filled with the metal layer **144**. Note that this means that it is the damascene interconnects **144** and not the vias for this level that connect downward to the contact plugs **128**. Subsequently, the via for this level will be formed in the upper portion of the damascene interconnects **144** making this a reversed damascene process when compared to the typical prior art. Note also that the damascene interconnects **144** are truly formed by a damascene process comprising trench formation followed by metal inlay. Therefore, the entire thickness of the metal layer does not have to be etched in the interconnect formation process.

Referring now to FIG. **6**, the damascene interconnects **144** are patterned to form via plugs **152**. This patterning is done by a photolithographic process. An organic bottom anti-reflective coating (BARC) layer **149** is applied overlying the metal layer **144**. The BARC layer **149** reduces the reflectivity of the metal layer **144** during the exposure step of the lithographic sequence. The BARC layer **149** comprises a commercially available material such as poly (arylsulfonate)-based material or polyacrylate-based material. It should be understood that the BARC layer **149** is an optional step that is included in the present invention as a typical process. A photoresist layer **148**, **152** is applied overlying the BARC layer **149**. The photoresist layer **148**, **152** is exposed to actinic light through a mask that combines the data of the aforementioned trench mask (photoresist areas labeled **148**) with data specific to the via plugs (photoresist areas labeled **152**). After development, the photoresist layer **148**, **152** remains overlying the first dielectric layer **132** and the damascene interconnects **144** while exposing a selected part of the damascene interconnects. The presence of the photoresist layer **148** overlying the first dielectric layer **132** protects the first dielectric layer **132** from metal diffusion, especially of copper, during the etching process.

Note that the patterned photoresist layer sections **148** and **152** may need to be oversized to insure that the first dielectric layer **132** is never exposed during the etching of the metal layer **144**. For example, if an anisotropic dry etching process is used to etch the metal layer **144**, then the patterned photoresist sections **148** should be oversized on the trench edge **150** by between about 0.01 microns and 0.5 microns to insure that the patterned photoresist **148** overlaps the conductive barrier layer **140** even under worst case alignment. If a wet etch is used, then the patterned photoresist sections **148** should be oversized on the trench edge **150** by between about 0.01 microns and 0.5 microns and the patterned photoresist section **152** overlying the via plugs **160** should be oversized **151** by between about 0.02 microns and 1.0 micron to compensate for alignment tolerance and for lateral etching that may occur. These concepts are also applicable for subsequent levels of damascene interconnects formed in the method of the present invention.

The patterning of the damascene interconnects **144** is accomplished by plasma-assisted dry etching or by wet etching. A wet etching selective to the metal layer **144** relative to the conductive barrier layer **140** is preferred. If a wet etch is used and the metal of the metal layer **140** is copper, the etching chemistry should comprise one or more of the group containing: dimethylsulfoxide (DMSO), carbon tetrachloride (CCl_4), acetic acid (CH_3COOH), NH_4F, hydrofluoric acid (HF), tetramethylammonium hydroxide (TMAH), tetraethylammonium hydroxide (TEAH), tetrapropylammonium hydroxide (TPAH), water, surfactant, and benzotriazole (BTA). Some preferred solutions include: DMSO and CCl_4, NH_4F and acetic acid, and HF, NH_4F, and water. If a plasma-assisted dry etch is used, the etching chemistry should comprise one or more of the group containing: Cl_2, BCl_3, N_2, and fluorocarbons.

The etching process is timed such that the damascene interconnects **144** are only partially etched down. After the etch, via plugs **160** have been formed in an upper portion of the damascene interconnects **144**. The remaining lower portion may now be called the conductive lines **156**. Note that the via plugs **160** are formed from the same metal layer **144** as the conductive lines **156**. Therefore, there is no possibility of the via plugs **160** being misaligned to the conductive lines **156**. Preferably, the via plugs are formed with a vertical thickness of between about 2,000 Angstroms and 10,000 Angstroms.

The presence of the conductive barrier layer **140** and the photoresist layer **148** overlying the first dielectric layer **132** prevents metal contamination, especially copper, into the first dielectric layer **132** during the etching process. Upon removal of the photoresist layer **148** and **152**, an optional hydrogen plasma or ammonia plasma treatment may be performed to remove any copper oxide from the surface prior to the deposition of the next layer of film.

Referring now to FIG. **7**, a non-conductive barrier layer **164** is deposited overlying the first dielectric layer **132**, the conductive barrier layer **140**, the via plugs and the conductive lines **144**. There are two purposes for the non-conductive barrier layer **164**. First, if copper is used for the metal layer, the non-conductive barrier layer **164** prevents copper ion diffusion into the overlying dielectric material. Second, the non-conductive barrier layer **164** can act as an etch stop during formation of trenches for the next level of interconnect. The non-conductive barrier layer **164** comprises one or more of the following materials: silicon nitride, Applied Material Corporation's BLok, silicon carbide, carbon nitride, boron nitride, carbon boron nitride, and silicon oxynitride. The non-conductive barrier layer **164** is preferably deposited to a thickness of between about 50 Angstroms and 5,000 Angstroms.

A second dielectric layer **168**, **172** is deposited overlying the non-conductive barrier layer **164**. The second dielectric